# A Monolithic Preamplifier-Shaper for Measurement of Energy Loss and Transition Radiation*

A. Kandasamy[1], E. O'Brien[1], P. O'Connor[1], and W. Von Achen[2]
[1]Brookhaven National Laboratory, Upton, NY 11973
[2]Rensselaer Polytechnic Institute, Troy, NY 12180

*Abstract*

A custom monolithic circuit has been developed for the Time Expansion Chamber (TEC) of the PHENIX detector at the Relativistic Heavy Ion Collider (RHIC) at Brookhaven National Laboratory (BNL). This detector identifies particles by sampling their ionization energy loss (dE/dx) over a 3 cm drift space and by detecting associated transition radiation (TR) photons. The requirement of being simultaneously sensitive to dE/dx and TR events requires a dual-gain system.

We have developed a compact solution featuring an octal preamplifier/shaper (P/S) IC with a split gain stage. The circuit, fabricated in 1.2 μm CMOS process, incorporates a trans-impedance preamplifier and a 70 ns unipolar CR-RC$^4$ shaper with ion tail compensation and active DC offset cancellation. Digitally selectable gain, peaking time, and tail cancellation as well as channel-by-channel charge injection and disable can be configured in the system via a 3-wire interface. The 3.5 x 4.5 mm$^2$ die is packaged in a fine pitch 64-pin PQFP. Equivalent input noise is less than 1500 rms electrons at a power dissipation of 30 mW per channel. On a sample of 2400 chips, the DC offset was 2.3 ± 3 mV rms without trimming.

A chamber-mounted TEC-PS Printed Circuit Board (PCB) houses four P/S chips, on-board calibration circuit, and 64 analog differential line drivers which transmit the shaped pulses to crate-mounted flash ADC's 7 m apart. An RS-422 link provides digital configuration downloading and read back, and supplies the calibration strobe. The 24.6 cm x 9.5 cm board dissipates 8.5 W.

## I. INTRODUCTION

### *Time Expansion Chamber*

The TEC of the PHENIX experiment (Figure 1), provides charged particle track information between the Ring Imaging Cherenkov detector and the Electromagnetic Calorimeter subsystems and contributes to the electron-pion discrimination of the entire PHENIX detector by performing fine sampling dE/dx measurements [1].

As the charged particle passes through the chamber (Figure 2), the electron clusters formed by the ionization of the gas drift toward the anode wires where charge amplification occurs. The signal from each anode wire is read out through a preamplifier-shaping amplifier and then digitized to determine the time profile and the pulse height of the signal.

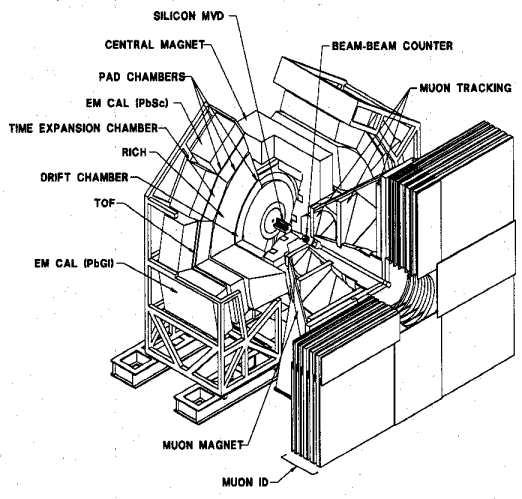


Figure 1. PHENIX detector.

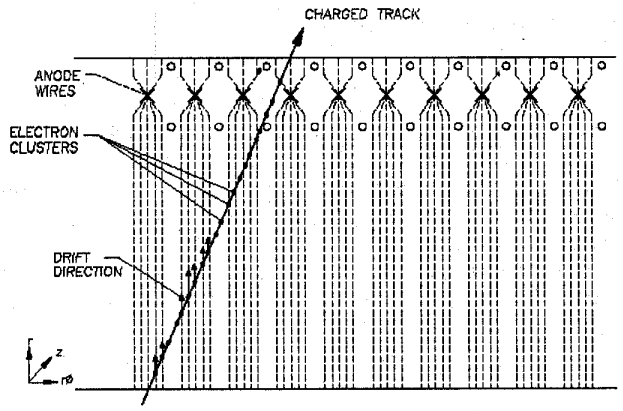


Figure 2. Time Expansion Chamber showing anode/cathode configuration, electric field lines and drift direction of electron clusters created by ionizing particles.

The TEC in its final configuration will consist of six planes of tracking, energy loss measurement and TR with Xe based gas mixture. The proposed channel count for the TEC is 43,250 electronic channels.

## II. SYSTEM REQUIREMENTS

Minimum ionizing particles deposit about 0.16 keV/mm in the gas. Taking into account the drift velocity, gas gain, and

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effective integration time of the shaper (70 ns), this corresponds to 8 fC of charge into the preamplifier per 70 ns "time slice". For this input signal, adequate electron-pion separation can be achieved with an equivalent input noise charge (ENC) of 1500 rms electrons.

The P/S must not saturate when a TR photon deposits up to 10 keV (300 fC) in a single "time slice". To accommodate this large dynamic range, we developed a dual gain system. The signal is split after the shaping amplifier and two outputs are provided, with nominal gain of 25 and 5 mV/fC for the dE/dx and TR measurement, respectively.

After amplification, the pulses are sent to a nonlinear flash ADC which digitizes both the dE/dx and TR signals at 40 Msamples/s and encodes the result into a 5-bit value [2]. We measure about 80 samples of the deposited charge along the drift space of the TEC. This allows good statistical analysis of the energy loss for particle identification, provides tracking information, and identifies transition radiation if present.

## III. ARCHITECTURE

The block diagram of a single preamplifier/shaping amplifier is shown in Figure 3. It consists of a 75 kΩ trans-impedance stage followed by four active stages for shaping and gain. Each stage has digitally controlled capacitor and resistor arrays to adjust time constants and gain ratios. Since the entire preamplifier is DC coupled, offsets are controlled using two active feedback loops with long time constants. This is equivalent to AC coupling the stages. Each channel has an on-chip charge injection capacitor that can be switched into the input of the preamplifier for calibration. Each channel also has the capability to be powered down in case of excessive noise in the channel.

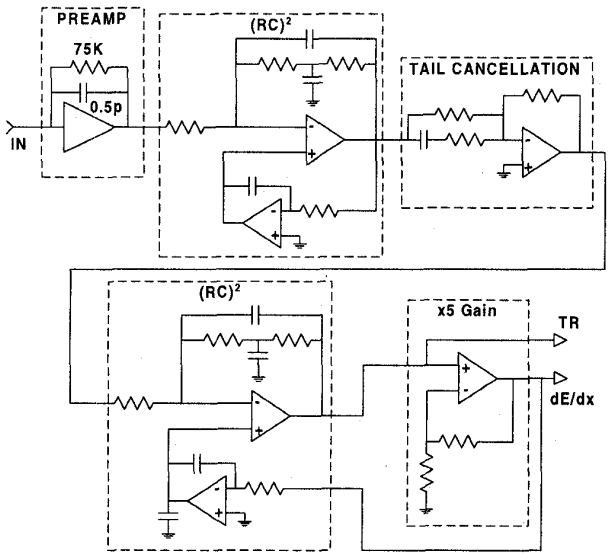


Figure 3. TEC P/S block diagram.

The P/S ASIC is realized in a 1.2 micron n-well CMOS, double-metal process.

### *1. Preamplifier*

The TEC current sensitive preamplifier [3] shown in Figure 4, is a folded cascode topology, with an NMOS input device (W/L=4200/1.2), drain current of 600 μA and $g_m$=12 mS. The feedback capacitor is realized as an N+ active - polysilicon, linear capacitor of 1.15 fF/μm$^2$.

The preamplifier also provides the first stage of shaping. By selecting $R_fC_f < T_m$, ($T_m$ being the shaping time of the preamp) the system's impulse response has approximately equal rise and fall time, thus eliminating the need of an additional preamp tail cancellation stage. The resistor $R_f$ is realized using polysilicon (R ≈ 27 Ω/square). The front-end designed for the TEC has to provide a linear response for dE/dx up to 100 fC in a 70 ns time slice.

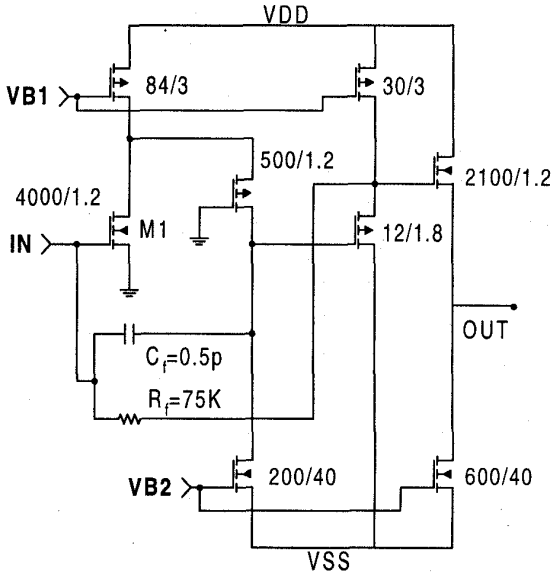


Figure 4. Current sensitive preamplifier.

The gain of the current-sensitive preamplifier in terms of input charge are given in Equations 1,2 and 3.

$$V_o \cong I_{in} \bullet \left(\frac{T_d}{T_m}\right) \bullet R_f \qquad (1)$$

$$V_o \cong Q_{in} \bullet \frac{R_f}{T_m} \qquad (2)$$

$$Gain \cong \frac{V_o}{Q_{in}} \cong \frac{R_f}{T_m} \qquad (3)$$

Where,

$V_o$ = output of the preamplifier

$I_{in}$ = detector current.

$R_f$ = feedback resistor

$T_m$ = Shaping time.

$T_d$ = Total current collection time.

## 2. Shaping amplifier

Two bridged-T type active stages provide the required 70 ns semi-Gaussian CR-RC$^4$ shaping. The feedback capacitors of the bridged-T are an array of capacitors that can be switched in and out of the network by CMOS switches. Two digital lines provide four steps of shaping to compensate for about ±20% process variation.

The operational amplifier used in the active stages of the shaping and gain stage is a two stage CMOS Miller output trans-impedance amplifier type [4,5]. The unity gain frequency of the opamp is 70 MHz and the open loop gain is 60 dB. The power dissipation of the opamp is 6.25 mW.

As the entire P/S chain is DC coupled, the offset is compensated by a DC re-balancing feedback circuit in the active filter stages, see Figure 5. The input resistance of the integrator is a "floating active resistor" realized using a long channel pmos device, biased in the weak inversion region. This provides the required time constant of several hundred microseconds.

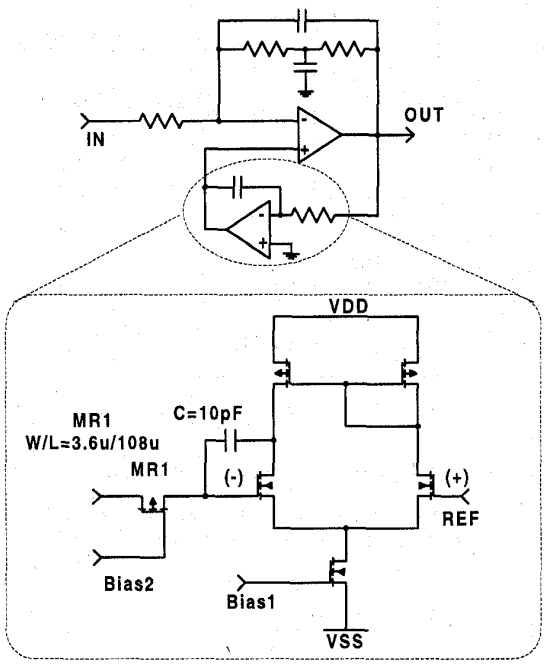


Figure 5. AC coupling by an integrator in feedback.

## 3. Ion tail cancellation

The long positive ion tail current from proportional chambers [6] causes a slow return to baseline. A variable tail cancellation [6,7] stage has been realized in the shaping amplifier chain allowing the electronics to be used in a variety of gas mixtures with different ion mobility. A single digitally controlled time constant is used in the chip.

## 4. Output gain stage

After the final shaping stage, the signal is split. A non-inverting active gain stage based on the shaper opamp provides a fixed gain of 5 for the dE/dx output. The output of the shaper provides the low-gain TR output.

The bandwidth of the gain stage is high enough to preserve the 70 ns rising edge of the shaped pulse.

Gain control of the shaping amplifier is provided by a programmable resistor array in the second stage of the shaper. There are a total of eight gain steps for the outputs. Some change to the pulse shape is seen at different gains.

## 5. Calibration and channel enable

Each P/S channel has an on-chip charge injection capacitor ($C_c$ = 0.5 pF) at its preamp input. These capacitors can be switched in and out of the circuit on a channel-by-channel basis.

The power dissipation of each preamp-shaper channel is 11 mW when disabled and 30 mW when enabled.

## 6. Serial link

The TEC P/S chip has a 24-bit shift register that is used for storing the configuration variables of the chip. As described previously, the preamp shaper channels have 8 steps of gain tuning, 8 steps of tail cancellation settings, 4 steps of shaping time settings, calibration mask and channel enable mask. The control lines for these settings provide the variable configuration of the chip. Channel calibration and channel enable masks are individually controlled for every channel, whereas the gain, shaping and tail cancellation settings are global for the entire chip.

The shift register is of the type, serial-in serial-out with parallel load capability. The serial-out line can be used to daisy chain more preamp-shaper chips together. This serial link requires a 3-wire interface to the external world for downloading the configuration data. The configuration registers can be pin-programmed to a default state for use without the serial link.

## 7. Bias generators, power distribution and input protection

The architecture of the octal TEC P/S CMOS monolithic circuit is shown in Figure 6. The die consists of 8 P/S channels, five bias voltage generator circuits for the current mirrors in the preamplifier, opamp and integrator. The input-output pads contain electro-static discharge (ESD) protection circuits, and the digital lines have buffered I/O pads.

The floor plan of the chip subdivides the channels into two banks of four channels each. The power for the chip is divided into four groups. Each bank of channels has its preamplifier power separate from its shaper counterpart.

The TEC CMOS monolithic integrated circuit has been produced in Hewlett-Packard's 1.2 μm N-Well CMOS34/AMOSI technology with linear capacitor. The layout of the production chip is shown in Figure 7. The size of the die is 3.4 mm x 4.5 mm.

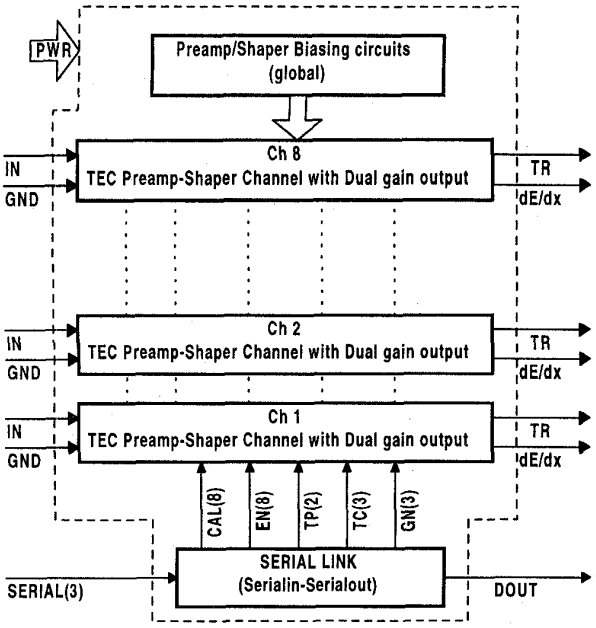


Figure 6. Octal TEC P/S block diagram.

The die is packaged in a fine pitch (19 mil), 10 mm x 10 mm, 64-pin quad flat plastic package. The 20 wafer production run yielded 14,000 packaged chips.

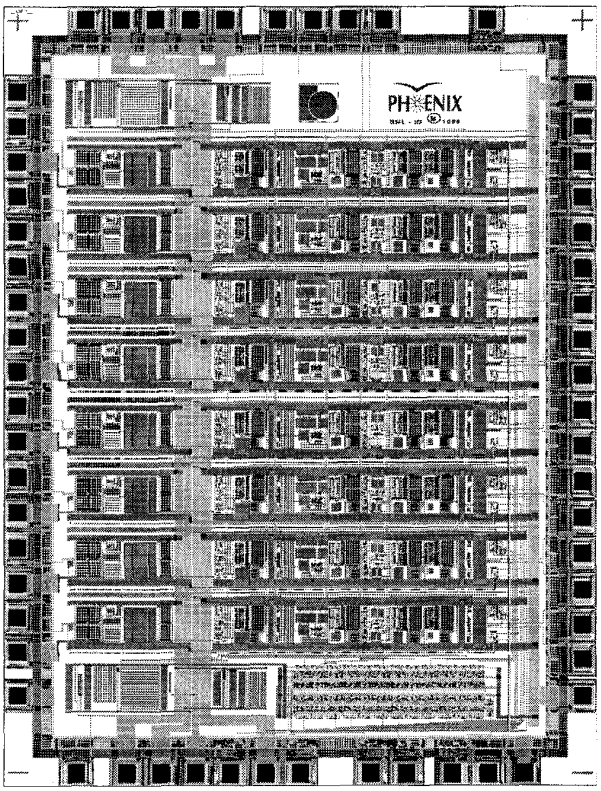


Figure 7. Octal TEC P/S chip.

## IV. Testing and Performance

A large sample of the packaged chips were tested using an automated test fixture. We have studied the performance of the chips with both prototype and production chambers.

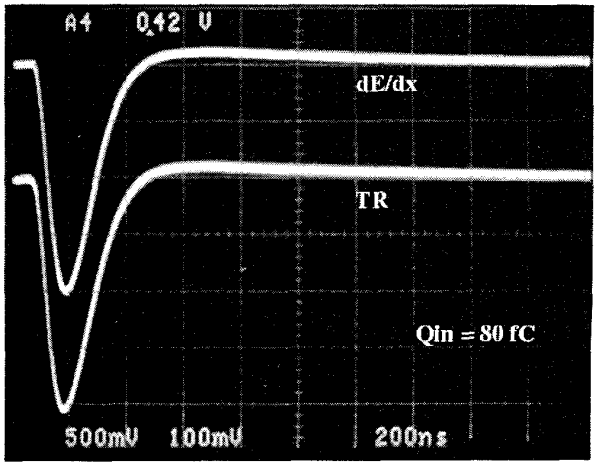


Figure 8. Impulse response of the P/S.

The impulse response of a P/S channel is shown in Figure 8, obtained by applying a step input corresponding to 80 fC of charge to the internal charge injection capacitors.

The chip was assembled into a TEC-PS PCB and was tested with the chamber. The response of the P/S to $^{55}$Fe X-ray photons of 5.9 keV is shown Figure 9. Both 5.9 keV and the argon escape peaks are visible.

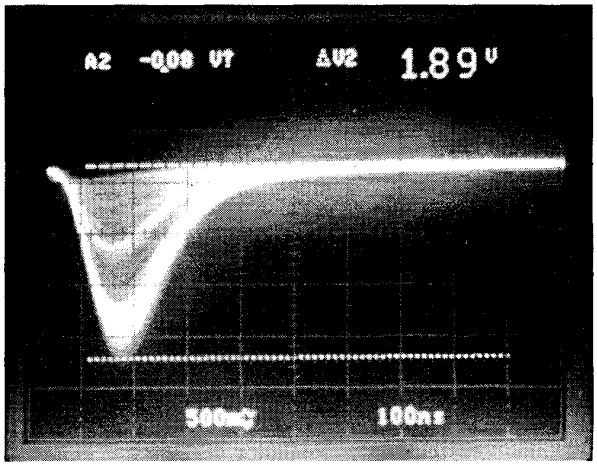


Figure 9. TEC-P/S output response to $^{55}$Fe source incident on the TEC filled with P-10 gas.

### *1. Automated test fixture*

The test fixture consists of a set of multiplexers for selecting the channel under test and also other items, such as bias lines and power supply voltages. Also included are: a serial digital-to-analog (DAC) converter for setting the window comparator limits, a dual comparator for measuring the pulse height, a serial ADC for measuring DC voltages and a programmable delay line for determining the output pulse

width, as well as other auxiliary devices like voltage reference, oscillator etc.

The hardware is interfaced to an IBM PC parallel port and the control and data acquisition software is written in Power BASIC. The output pulse height is determined by coarsely hunting for the peak using the window comparator and then by means of a fine step search. The delay line along with a D flip-flop and the comparator is used for determining the output pulse width at a specified fraction of the pulse height. The entire setup requires two printed circuit boards. The test fixture also measures the supply current drawn by the device under test (DUT). The first PCB houses the clamshell socket for the DUT, and the second PCB contains the hardware that interfaces to the PC. We record peak height, pulse width, offset and noise of the 16 outputs, along with the DC bias voltages and power supply currents for the chip. Running time is about 25 seconds per chip limited by the throughput of the PC parallel port.

A total of 2452 P/S chips (19,200 channels), sufficient for the first TEC-PS PCB production run were tested using this fixture and the results are summarized in Table 1. $T_{shaping}$ is defined as 1% to 99% rise/fall time of the pulse. The chips were measured with the configuration registers in their default state. The production chips exhibit longer $T_{shaping}$ than the prototypes. The serial link can be used to program the registers for 70 ns $T_{shaping}$ in system.

| Signal | Parameter | Mean | Std. Dev. |
|---|---|---|---|
| dE/dx | Gain(mV/fC) | 26.1 | 5.0% |
| | Tshaping (ns) | 95.4 | 2.8% |
| | Offset (mV) | -2.3 | 2.6 |
| TR | Gain(mV/fC) | 5.4 | 5.3% |
| | Tshaping (ns) | 97.4 | 3.4% |
| | Offset (mV) | -3.0 | 1.6 |
| Power | Pdiss (mW)/Ch | 29.9 | 3.2% |

Table 1. Results of 19200 channels tested.

The gain linearity of the dE/dx signal is shown in Figure 10. The measured integral non-linearity (INL) for dE/dx is less than 1% and for the TR is less than 3%.

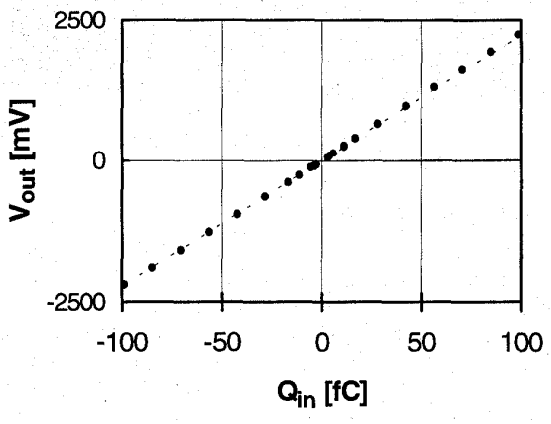


Figure 10. dE/dx gain of TEC-PS.

A total of 52 chips failed, for a yield of 97.8%. The main failure modes are summarized in Figure 11.

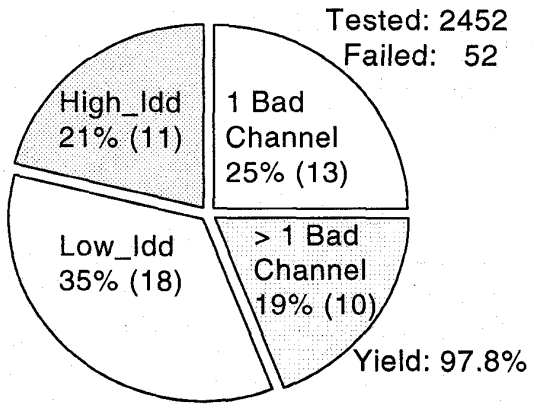


Figure 11. Failure modes.

## 2. *ESD susceptibility testing*

The P/S chip have protected I/O pads on all of its terminals. This I/O pad has two field oxide devices and two field plated diodes. The digital lines have a 200 Ω resistor in series with their inputs.

The P/S chip was tested for its susceptibility to electro static discharge. The test was performed by exciting the inputs of the preamplifier with 100 μJ of energy at a rate of 1 Hz. The test fixture consists of a storage capacitor (47 pF) connected to a 1.5 kV voltage source through a 1 MΩ resistor. A high voltage relay was used to discharge the stored energy. The DUT was decoupled from the storage capacitor by a 470 pF capacitor. This simulates the scenario that arises from a broken wire in the chamber. The internal protection devices were sufficient to guard the inputs for about ten such events. The channels were tested with additional external protection diode/resistor network. With external protection network the chip sustained over 1000 discharges with no failures.

## V. PREAMPLIFIER/SHAPER BOARD

The block diagram of the P/S board is shown Figure 12. The principal components of this board are:

- Four octal P/S chips.
- Differential line drivers for the 64 output signals (32 Channels x 2 gains)
- Common calibration DAC and control logic.
- RS-422 serial interface.
- Linear power regulation, filtering and fuses.
- External ESD protection for preamp inputs.

The TEC-PS PCB contains local low drop-out regulators for onboard power regulation along with supply filtering circuits. The electronics in the TEC-PS PCB are protected from over current by means of poly-resettable fuses and by reverse biased power diodes for input voltage reversal protection. An onboard 12-bit DAC is used for providing

precision voltage levels for calibrating the 32 P/S channels. The four octal P/S chips are daisy chained using their serial lines, such that configuration data can be downloaded in a single data stream. The data stream consists of 108 bits, 96 for the P/S chips and 12 for the calibration DAC. The serial data is received over the twisted pair cable from the front-end-module as differential RS-422 level signals. The TEC-PS PCB has provisions for the downloaded data stream to be read back for verification purposes. The read back data also follow RS-422 signaling.

A prototype version of the TEC-PS PCB was tested in the test beam of the Alternating Gradient Synchrotron facility at BNL [8,9]. The cross talk measurement performed indicates the P/S channel in the TEC-PS PCB has less than 2% cross talk to its neighbors.

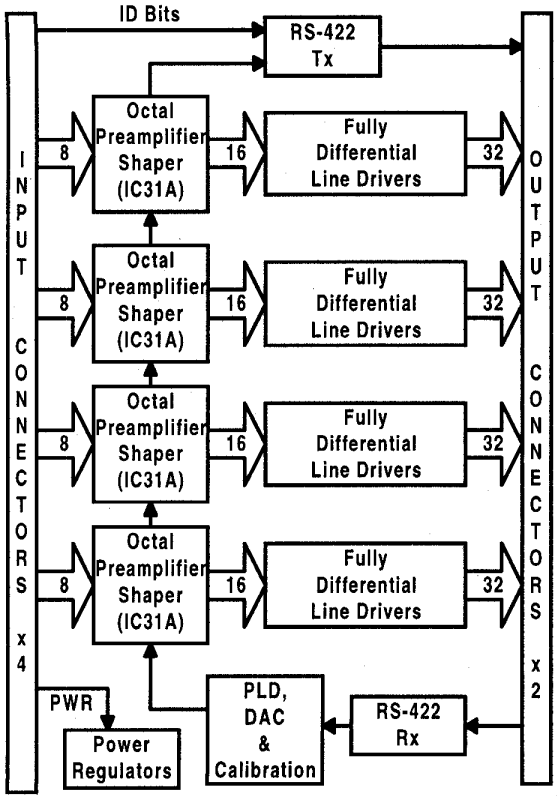


Figure 12. Thirty-two channel preamp/shaper PCB.

## VI. CONCLUSION

A monolithic CMOS octal P/S chip for measurement of energy loss and transition radiation has been developed. Five hundred, 32 channel front end printed circuit boards using the octal P/S chip have been fabricated and are scheduled for assembly and installation into the PHENIX Time Expansion Chamber in 1999. The parameters of both the octal P/S chip and the 32 channel P/S printed circuit board are summarized in Table 2. Production testing of 5,000 P/S chips and 500 TEC-PS PCB's is scheduled to be completed by the end of 1999.

| Preamplifier/Shaper ASIC | |
|---|---|
| Inputs | 8 |
| | Individual ground returns/channel |
| Input protection | Internal ESD protection pads |
| Outputs | 8 dE/dx ( x5 Gain) |
| | 8 TR (x1 Gain) |
| Gain | 5 mV/fC to 50 mV/fC (dE/dx) variable |
| Shaping | 60 ns to 110 ns variable |
| Ion tail cancellation | Variable |
| Noise @ 18pF,95ns | 1419 electrons rms (dE/dX) |
| | 1526 electrons rms (TR) |
| Linearity (INL) | < 1% (dE/dx) and < 3% (TR) upto 100 fC input charge. |
| Offset | Internal DC re-balancing with external offset trimming capability |
| Power | +2.5 V and -2.5 V |
| Power dissipation | 30 mW/channel |
| Die size | 3.39 mm x 4.49 mm |
| Process | 1.2u N-well CMOS34/AMOSI/Linear-capacitor |
| Foundry | Hewlett Packard |
| Package | ASAT-Wales,U.K./64pin PQFP (10mm x 10mm) |
| **Preamplifier/Shaper PCB** | |
| Inputs | 32 |
| Outputs | 32 dE/dx |
| | 32 TR |
| Output type | Fully differential |
| Protection circuits | External diodes on preamp inputs |
| | Poly-resettable fuses on power-supplies |
| | Input reverse voltage protection |
| Power | +6 V and -6 V |
| Power dissipation | 262 mW/channel |
| Board size | 24.6 cm x 9.5 cm |

Table 2. Summary of P/S chip and PCB.

## VII. ACKNOWLEDGMENTS

The authors gratefully acknowledge the many fruitful technical discussions with R. L. Chase, J. A. Harder and V. Radeka. Also R. Machnowski, J. Triolo and K. Wolniewicz for their technical expertise in printed circuit board layout and assembly and W. Chang, A. Franz, D. Kotchetkov, M. Munirzamman, R. Pisani, M. Rosati, R. Seto and H. Wang for their immense help in testing.

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